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How do Topological Properties of Ripple-Carry Adders Affect Time Delay?

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Abstract

This poster presents topological properties of N-bit ripple-carry adders and the effects of their topology, specifically their genus, on the speed of current flow. An adder is a very simple computer that takes input numbers (0 and 1) from logic gates and then adds them together. To create a ripple-carry adder, we take N number of adder circuits and arrange them in parallel. We differentiate between two kinds of adder circuits: half adders and full adders. Half adders are non-planar (has loops) circuits with genus = 1 that let us perform elementary addition operations using logic gates. Full adder circuits are non-planar circuits with genus = 2 that comprise three inputs (A, B, and the Carry input) and two outputs (Sum and the Carry output), sending the carry input from one adder to the next. We can think of the genus of a circuit as the number of loops a surface needs in order for a circuit to be drawn on it without any crossings.

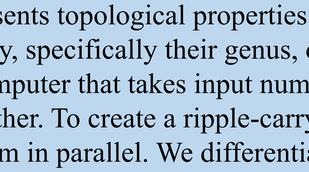
Introduction

We hypothesized that if we increase the number of bits, then the speed for the ripple-carry adder would decrease (time delay become maximized) as well because a circuit with more pieces has longer routes for current to flow. It had previously been shown by Sam Swanson's research that the genus of an N-bit ripple-carry adder increases as the number of bits increases. This led to us thinking that there must be a direct relationship between the genus of a N-bit ripple-carry adder circuit and the speed of the circuit's current flow. From this we thought that we could construct ripple-carry adder circuits that maximize the speed of current flow while using fewer bits.

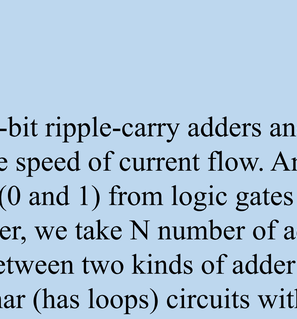
Method

First, we constructed a truth table.

A	B	C_{in}	C'	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Example of 1-bit Ripple-Carry Adder



Example of 2-bit Ripple-Carry Adder

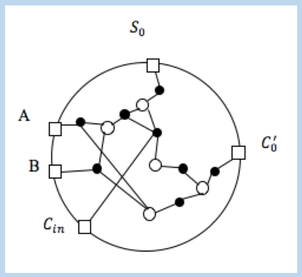
Next, we constructed a 1-bit and a 2-bit ripple-carry adder circuit simulation using OrCAD. We began by considering a 1-bit full adder with inputs A, B, a carry-in bit C, and outputs called Sum and Carry. Next, we constructed a 1-bit ripple-carry adder using OrCAD Capture CIS. First, we created a schematic design of our ripple-carry adder circuit. This is done by first opening up a schematic design template and adding necessary circuit parts and wires. We processed our design using part references and prepared our design for simulation. Following that, we created and edited a simulation profile. This was followed by running the simulation. From here, we added in any resistors and capacitors, connecting them with the wire bridging 2 adjacent full ripple-carry adders. Then, we constructed a 2-dimensional circuit map for each adder circuit. We tracked the number of vertices, edges, and faces of each circuit. For each of the ripple-carry adder circuits, we created a circuit map detailing the vertices and edges.

Method Continued

From this we calculated the genus. Following that, we added a resistor to each of the circuits in the OrCAD simulation and experimented with varying the resistance in the ripple-carry adder circuits to see how that affects the time-delay of the current flow. Finally, we used Microsoft Visio to create models of the circuits we simulated in OrCAD.

Results

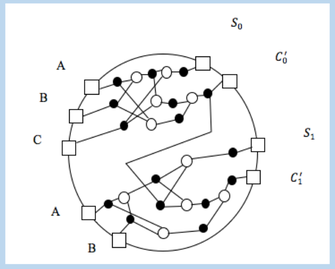
Topological properties were extracted for ripple-carry adders constructed from full adder cells. Two ripple-carry adders with N = 1 bit and two with N = 2 bits are shown. The genus calculated from each circuit is shown in the table. The results show that the genus equals 2N, where N is the number of bits in a ripple-carry adder. The worst-case delay in a ripple-carry adder is proportional to the number of bits N. This is because the carry-input bit propagates from the least significant bit position all the way to the most significant bit. Furthermore, the results indeed show that as the genus is increased, the time delay increases proportionally.



1-bit Ripple-Carry Adder with XOR,AND,OR gates

g = 2

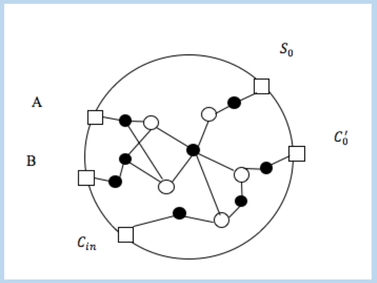
Time Delay for the above 2-bit ripple-carry adder = 5.0275us



2-bit Ripple-Carry Adder with XOR,AND,OR gates

g = 2

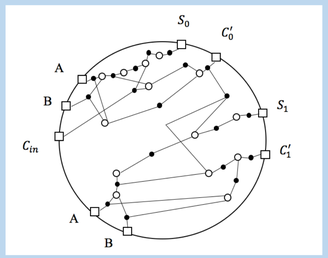
Time Delay for the above 2-bit ripple-carry adder = 10.0550us



1-bit Ripple-Carry Adder with NAND, AND, OR gates

g = 4

Time Delay for the above 2-bit ripple-carry adder = 5.0420us



2-bit Ripple-Carry Adder with NAND, AND, OR gates

g =4

Time Delay for the above 2-bit ripple-carry adder = 10.0840us

Summary/Conclusions

Research in the area of topological constraints and their effects extends previous work that sought how the genus value changes as the number of bits is increased for ripple-carry adder circuits. For any N-bit ripple-carry adder, the genus as studied in this research, is equal to 2N. We found that using fewer bits we can maximize the speed, and therefore minimize the time delay of current flow. The results show that as the genus of a ripple-carry adder circuit increases, so does the time delay of the device.

Acknowledgements

I would like to acknowledge Dr. Lanzerotti and Dr. Engebretson for their roles in advising me in my research, Eric Strom in helping with technical issues surrounding OrCAD software, and Alex Sushko (an alumnus) for giving me pointers in the construction of ripple-carry adders.

Future Work

Future work will focus on extracting topological properties and their effects on the time delay of current flow of increasingly complex integrated circuits.

References

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